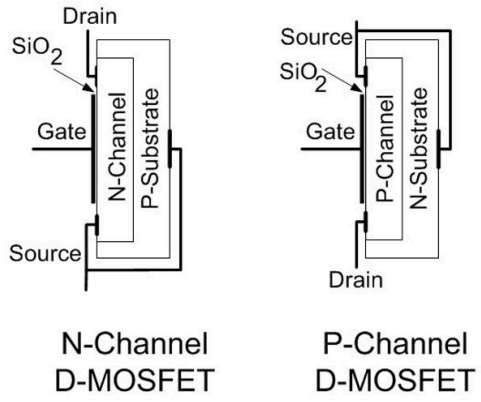
Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

Remember our analogy of comparing a mouse to a very large beetle? One of the biggest differences between the two, biologically, is that one is a vertebrate, and one is an invertebrate. However, when it comes to invertebrates, there are differences that are even more extreme than between the mouse and the beetle -- there are worm-like invertebrates, insect-like invertebrates, starfish-like invertebrates, clam-like invertebrates, and so on. The same is true, in a sense, for Field Effect Transistors.

A very different configuration for controlling a single channel of semiconductor material was invented, and the result is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). And, it this general category, there are a number of types of devices, generally arranged in two groups -- D-MOSFET and E-MOSFET.

D-MOSFET

We'll start with the Depletion and Enhancement MOSFET, because this will help us understand how the E-MOSFET works; the D-MOSFET isn't even a transistor you can buy as a component, so it's not something you will likely ever have any experience with. But unless you understand the concept of Enhancement, the operation of the E-MOSFET, which makes up by far the bulk of the transistors ever made, will be a mystery.



As with the JFET, the Drain and Source are connected to the two ends of one piece of material, which becomes the channel. However, unlike the JFET, the Gate is not connected to the other semiconductor material. Instead, it is simply a piece of metal separated from the channel by a thin layer of oxidized silicon, SiO_2, which is the same material sand is made of, and is a really good insulator. This is where the name comes from: Metal to Oxide to Semiconductor FET.

The biggest difference between the JFET and the MOSFET is that forward-biasing the Gate to Source potential does not turn this device into a poor diode, as it would have done in the case of the JFET, because no current can flow through the insulating layer at the Gate. Therefore, there is no "forbidden voltage range", other than going beyond the maximum voltages possible for the device.

There is a second metal connection that keeps the Substrate potential the same as the Source potential. This way, as V_{GS} changes, an electric field, or potential, is developed across the P-N junction without a physical connection to the Gate.

As with the JFET, when the P-N Junction is reverse-biased, the depletion region increases in thickness, reducing the Channel and thereby reducing the current. At some point, the Channel will be reduced to nothing, and the Channel will be turned off. As with the JFET, this will be V_{GSoff}.

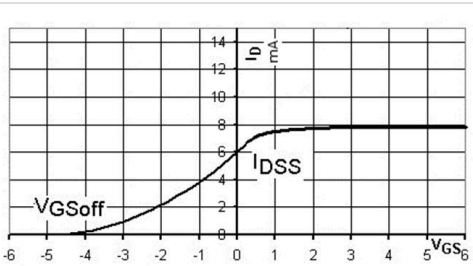
When V_{GS}=0, again a large amount of current will flow, and this will be called I_{DSS}. Incidentally, the term means "I_D when the Gate is Shorted to the Source", which is how they determine what I_{DSS} is. Of course, that same amount of current flows when the Gate and Source voltages are the same, whether or not they are physically shorted together.

However, in the case of the D-MOSFET, this isn't the maximum current that can flow, because we can take V_{GS} to the other side of the y-axis, since forward biasing doesn't damage the transistor. When we do this, the depletion region is actually decreased, which results in the widening of the channel, in turn resulting in more current than I_{DSS} flowing through the device. This widening of the channel is called ***Enhancement***. Enhancement can extend past simply reducing the depletion region to zero -- by forcing carriers of the opposite kind into existing semiconductor material, it can actually make a region of N-Material behave like P-Material or *vice versa*.

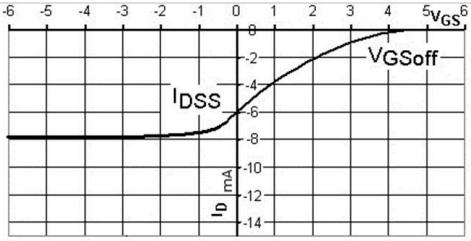
- ***Depletion*** referred to reducing the current by increasing the depletion region
- ***Enhancement*** refers to increasing the current by decreasing the depletion region and even pushing carriers past the original physical junction, creating new conductive material.

Consequently, this device is called the Depletion and Enhancement MOSFET, or simply D-MOSFET to try to keep the acronym small.

Here are the Transfer Functions for the only D-MOSFETs this author could find any information on, and they are buried inside an Integrated Circuit.



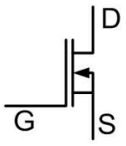
N-Channel D-MOSFET



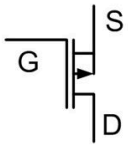
P-Channel D-MOSFET

Not very pretty -- most textbooks will show the enhancement-side of these curves as being a nice continuation of the parabola, but this doesn't appear to be the case. However, it shows that I_{DSS} and V_{GS}=0 are not the limits of operation for D-MOSFETs.

In a schematic, the following symbols are used:



N-Channel D-MOSFET



P-Channel D-MOSFET

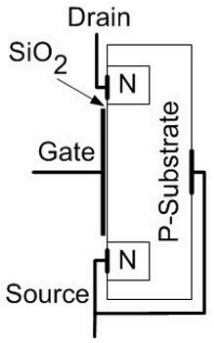
Again, the symbols are based upon the physical structure of the devices. The vertical bar is the channel, with metal connections to the Drain and Source. The Gate is shown as a metal layer physically separated from the channel by the thin layer of oxide, and the substrate connection indicates which material is P and which is N, with a metal connection typically between the Source and the substrate internal to the device.

Often, the Gate is shown with its connection close to the Source to remind us that V_{GS} is the controlling voltage.

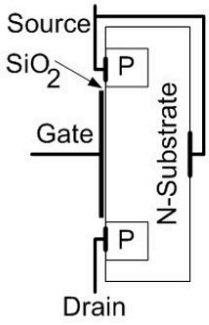
E-MOSFET

Finally! Now that we know what Enhancement is, we can get to the most common transistor ever made: the Enhancement-only MOSFET.

In an E-MOSFET, no channel exists in the resting state -- just two stubs of the channel material with a gap between them, filled with the substrate. This means that the P-N junctions around these stubs prevent the flow of current in the resting state, so, like the BJT, these devices are normally OFF, not ON as was the case for the JFET and the D-MOSFET.



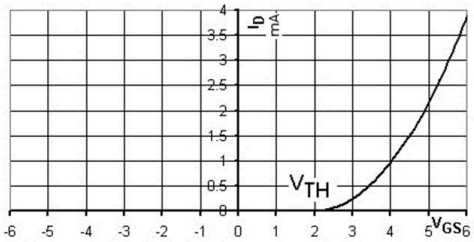
N-Channel
E-MOSFET



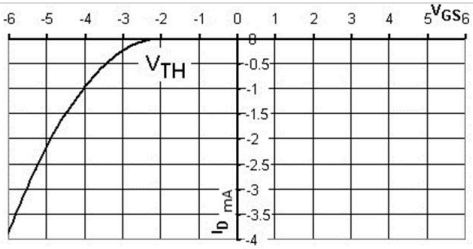
P-Channel
E-MOSFET

Of course, reverse biasing these devices would simply further turn them off, which has no effect. However, forward biasing the Gate to Source potential actually pushes the carriers in the substrate away from the Gate, eventually to the point where the substrate begins to behave as an extension of the stubs of the channel; a channel is created where no channel existed before, and current begins to flow.

The Transfer Characteristics show this effect:



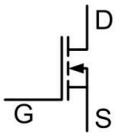
N-Channel E-MOSFET



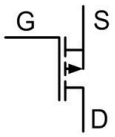
P-Channel E-MOSFET

Instead of V_{GSoff} we now have a threshold voltage, V_{TH} that must be overcome before the transistor will begin to conduct.

The schematic symbols for this device again show the physical characteristics of the device:



N-Channel E-MOSFET



P-Channel E-MOSFET

Notice that the Channels start off as broken lines -- they don't exist in the resting state, and only appear when the Gate to Source voltage is forward biased.

The E-MOSFET is more closely analogous to the BJT than the other FETs. Back to our biology analogy, we've come to, let's say, the octopus which, with its two big eyes and eight "legs" is more like the mouse than a clam would be; but they're really not at all related: they just both hide if you try to sneak up on them.

The E-MOSFET has the following characteristics that need to be considered when using it:

- Its output is non-linear, so it is best used as a switch rather than as an amplifier, unless it is used in a switch-mode (Class D) amplifier
- Its threshold voltage can be much higher than the 0.7 V required to turn on a BJT
- Its "On Resistance" is typically much lower than that of a BJT, usually in the milliohms
- Its "On Voltage" (V_{DSon}) is typically very close to zero, since there are no junctions to cross in the channel
- There is never any continuous Gate current, due to the insulating layer of SiO_2
- Unfortunately, the insulating layer is rather fragile, and can be damaged by Electrostatic Discharge (ESD), so FET devices need to be handled carefully and stored on static-dissipating foam
- Also unfortunate is the capacitance arising from the Gate-to-Channel separation, which results in an inrush current when the FET is turned on, a discharge current when the FET is turned off; the capacitance also may introduce a delayed response, since capacitors do not allow for instantaneous changes in voltage

Questions:

1. In one circuit, V_S = 0 V and V_D = +12 V. I_D increases continuously as V_G changes from negative to positive. What type of device is this? N-Channel D-MOSFET
2. In another circuit, V_S = 0 V and V_D = -9.0 V. When V_G = 0 V, no current flows. However, as V_G passes -2.4 V, current begins to flow. What type of device is this? P-Channel E-MOSFET
3. A technologist built a circuit using an N-Channel E-MOSFET. She applied +1.2 V between Gate and Source, but measured no current flowing through the Channel from Drain to Source. What is the most likely reason for this?

   VTH is apparently greater than +…
4. Our technologist from the previous question fixed her circuit. Being curious, she measured the Gate current. What do you predict she discovered? 0 μA